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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,816	06/23/2003	Heyun Howard Liu	TI-35745	7897

23494 7590 05/10/2011

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EXAMINER	
RHU, KRIS M	

ART UNIT	PAPER NUMBER
2184	

NOTIFICATION DATE	DELIVERY MODE
05/10/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)
	10/601,816	LIU, HEYUN HOWARD
	Examiner	Art Unit
	KRIS RHU	2184

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-35 and 37-41* is/are pending in the application.

4a) Of the above claim(s) *1-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-35 and 37-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)	
1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US 5,901,100) in view of Nagasawa (US 2003/0095787 A1) and Yeom et al. (US 6,282,203 B1.

Referring to claim 23, Taylor teaches a method of managing the communications of data words arranged in packets, the method comprising;

receiving a sequence of input data words at input terminals of the memory circuit **(Data IN 16, Figure 1)**;

receiving read strobe signals **("Writing and reading operations are controlled by 'write' and 'read' enables", Column 2, Lines 2-4)**; and

sequentially presenting the first and second output data words at output terminals of the memory circuit **(Data OUT 50, Figure 1; "a first-in, first-out ('FIFO') memory device 10 is shown", Column 3, Lines 66-67)**.

Taylor does not appear to teach each packet of data words including a start-of-packet indicator and an end-of-packet indicator; responsive to receiving a first input data word and a second input data word, performing a first width

conversion of the first and second input data words into a memory array of the memory circuit in a single write cycle; responsive to detecting the writing of input data words including a start-of-packet indicator and of an end-of-packet indicator, enabling the output of data words corresponding to the packet; responsive to receiving first and second read strobe signals, reading first and second output data words from the memory array in a single read cycle; and performing a second width conversion of the first and second output data words, wherein the first and second output data words are of the same word width as that of the input data words.

Nagasawa teaches responsive to receiving a first input data word and a second input data word, performing a first width conversion of the first and second input data words into a memory array of the memory circuit in a single write cycle **("In this embodiment, the transfer format of the data transferred from the external equipment not shown, is a serial transfer format in which one word has an eight-bit width. However, since the data is transferred on the data bus 30 by parallel transfer in which one word has a 16-bit width, the serial/parallel converting section 26 carries out serial/parallel conversion", Paragraph 0095, Lines 11-17; Thus, the words are written in parallel)**;

responsive to receiving first and second read strobe signals, reading first and second output data words from the memory array in a single read cycle **(Note the words are read in parallel)**; and

performing a second width conversion of the first and second output data words, wherein the first and second output data words are of the same word width as that of the input data words **("Similarly, the parallel/serial converting section 29 converts the parallel format in which one word has a 16-bt width to the serial format in which one word has an eight-bit width", Paragraph 0095, Lines 17-20)**.

Taylor and Nagasawa are analogous arts because they both teach buffering.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Taylor and Nagasawa before him or her, to modify Taylor to include responsive to receiving a first input data word and a second input data word, writing the first and second input data words into a memory array of the memory circuit in a single write cycle; and responsive to receiving first and second read strobe signals, reading first and second output data words from the memory array in a single read cycle, as taught by Nagasawa, because it merely would involve utilizing a known concept of deserializing received data before writing into of a FIFO and serializing data before reading out of a FIFO.

Therefore, it would have been obvious to combine Nagasawa with Taylor to obtain the invention as specified in the instant claim.

Yeom teaches each packet of data words including a start-of-packet indicator and an end-of-packet indicator **("The hardware router 21 checks the**

ninth bits and detects the start and end of the packet", Column 3, Lines 40-41), and responsive to detecting the writing of input data words including a start-of-packet indicator and of an end-of-packet indicator, enabling the output of data words corresponding to the packet **("Once the last byte of the packet is written to the transmitting buffer 220, the node 200 sends a packet ready signal, PKTRDY, to the hardware router 21", Column 3, Lines 41-44)**.

Taylor/Nagasawa and Yeom are analogous arts because they both teach buffering.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Taylor/Nagasawa and Yeom before him or her, to modify Taylor/Dobson to include each packet of data words including a start-of-packet indicator and an end-of-packet indicator, and responsive to detecting the writing of input data words including a start-of-packet indicator and of an end-of-packet indicator, enabling the output of data words corresponding to the packet because it merely would involve utilizing a known concepts of detecting the start and end of a packet and utilizing a packet ready signal as an enabling signal for enabling the output of data words once both the start and end of the packet has been detected to ensure that whole data words are written instead of partial words.

Therefore, it would have been obvious to combine Yeom with Taylor/Nagasawa to obtain the invention as specified in the instant claim.

As to claim 24, Taylor/Nagasawa/Yeom teaches the method of claim 23, wherein the method further comprises enabling the output of data words corresponding to the packet, responsive to detecting the writing of a start-of-packet indicator and to a packet size indicator indicating that the packet has a length greater than a threshold **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-16, Taylor; Note the clearing of the empty flag indicates that at least the start of one packet has been written into the FIFO memory, enabling reading from the FIFO memory)**.

As to claim 25, Taylor/Nagasawa/Yeom teaches the method of claim 23, further comprising: incrementing a count of the number of packets stored in the memory array responsive to detecting the writing of an end-of-packet indicator **(Write Row Counter, Column 6, Taylor)**.

As to claim 26, Taylor/Nagasawa/Yeom teaches the method of claim 25, wherein the method further comprises: disabling the outputting of output data words, responsive to the outputting of an end-of- packet indication for a packet and to the count indicating that no additional packets are stored **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-16, Taylor)**.

As to claim 27, Taylor/Nagasawa/Yeom teaches the method of claim 26, wherein the disabling step comprises controlling an output register to disable the presenting of output data words at the output terminals **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-16, Taylor)**.

3. Claims 28-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanna et al. (US 6,252,880 B1) in view of Taylor and Nagasawa.

Referring to claim 28, Hanna teaches a network node for controlling the transmission and receipt of packet- based data over a communications facility comprising:

a system interface **(Network Port 12, Figure 1)** that receives transmit data from a system **(Network Station 14, Figure 1)** and for outputting processed received signals to the system;

a transmit FIFO buffer **(Transmit FIFO Buffers 26, Figure 1)** that buffers transmit data received at the system interface;

a transceiver **(Network Port 12, Figure 1)** that drives the communications facility with transmitted signals corresponding to the transmit data, and that receives signals from the communications facility; and

a receive FIFO buffer **(Receive FIFO Buffers 24, Figure 1)** that buffers the received signals.

Hanna does not appear to teach each of the transmit and receive FIFO buffers including: a memory array; a clock terminal that receives a clock signal; a write enable terminal that receives a write enable signal; inputs that receive input data words; a read enable terminal that receives a read enable signal; outputs that presents output data words of the same word width as that of the input data words; a write buffer that is coupled to the inputs and to the array of memory

cells and that receives a sequence of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal, wherein the write buffer performs a first width conversion of the first and second input data words to the memory array in a single write cycle; read circuitry that requests a read of the memory array responsive to receiving first and second read enable signals at the read enable terminal; and a read buffer that receives first and second output data words from the memory array responsive to the request of the read of the memory array and that presents the first and second output data words in sequence to the outputs.

Taylor, however, teaches each of the transmit and receive FIFO buffers including:

a memory array **("The memory device 10 comprises, in pertinent part, a primary DRAM memory array", Column 4, Lines 1-2)**;

a clock terminal **(Write Clock 36 and Read Clock 38, Figure 1)** that receives a clock signal;

a write enable terminal that receives a write enable signal **("Writing and reading operations are controlled by 'write' and 'read' enables", Column 2, Lines 2-4)**;

inputs that receives input data words **(Data IN 16, Figure 1)**;

a read enable terminal that receives a read enable signal **("Writing and reading operations are controlled by 'write' and 'read' enables", Column 2, Lines 2-4)**;

outputs that presents output data words of the same word width as that of the input data words **(Data OUT 50, Figure 1; "The inputs and outputs 16, 50 are word-wide", Column 5, Line 29)**;

a write buffer **(Input Buffer 22, Figure 1)** that is coupled to the inputs and to the array of memory cells and that receives a sequence **(Note memory device 10 is a FIFO)** of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal;

read circuitry **(I/O and Control 42, Figure 1)** that requests a read of the memory array responsive to receiving first and second read enable signals at the read enable terminal; and

a read buffer **("the FIFO memory device 10 may also incorporate:...an output or multiple output buffers to enhance FIFO memory device 10 performance", Column 4, Line 65 to Column 5, Line 6, Taylor)** that receives first and second output data words from the memory array responsive to the request of the read of the memory array and that presents the first and second output data words in sequence **(Note memory device 10 is a FIFO)** to the outputs.

Hanna and Taylor are analogous arts because they both teach FIFOs.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Hanna and Taylor before him or her, to modify Hanna to include each of the transmit and receive FIFO buffers including: a memory array; a clock terminal that receives a clock signal; a write enable

terminal that receives a write enable signal; inputs that receives input data words; a read enable terminal that receives a read enable signal; outputs that presents output data words of the same word width as that of the input data words; a write buffer that is coupled to the inputs and to the array of memory cells and that receives a sequence of first and second input data words from the inputs in combination with corresponding write enable signals at the write enable terminal; read circuitry that requests a read of the memory array responsive to receiving first and second read enable signals at the read enable terminal; and a read buffer that receives first and second output data words from the memory array responsive to the request of the read of the memory array and that presents the first and second output data words in sequence to the outputs, as taught by Taylor, because it merely would involve substituting the FIFOs taught in Taylor for the FIFOs taught in Hanna.

Therefore, it would have been obvious to combine Taylor with Hanna to obtain the invention as specified in the instant claim.

Nagasawa teaches wherein the write buffer performs a first width conversion of the first and second input data words to the memory array in a single write cycle **("In this embodiment, the transfer format of the data transferred from the external equipment not shown, is a serial transfer format in which one word has an eight-bit width. However, since the data is transferred on the data bus 30 by parallel transfer in which one word has a 16-bit width, the serial/parallel converting section 26 carries out**

serial/parallel conversion", Paragraph 0095, Lines 11-17; Thus, the words are written in parallel).

Hanna/Taylor and Nagasawa are analogous arts because they both teach FIFOs.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Hanna/Taylor and Nagasawa before him or her, to modify Hanna/Taylor to include wherein the write buffer performs a first width conversion of the first and second input data words to the memory array in a single write cycle, as taught by Nagasawa, because it would merely involve utilizing a known concept of deserializing received data before writing to the receive FIFO.

Therefore, it would have been obvious to combine Nagasawa with Hanna/Taylor to obtain the invention as specified in the instant claim.

As to claim 29, Hanna/Taylor/Nagasawa teaches the network node of claim 28, wherein the transceiver further comprises:

a serializer **(Parallel to Serial Converter 29, Figure 1, Nagasawa)** that serializes the transmit data;

a line driver that drives the communications facility with serial signals from the serializer **(Serial Data line 33, Figure 1, Nagasawa)**;

a receiver **(input 32, Figure 1, Nagasawa)** that receives serial signals from the communications facility; and a deserializer **(Serial to Parallel**

Converter 26, Figure 1, Nagasawa), for deserializing the signals received by the receiver.

As to claim 30, Hanna/Taylor/Nagasawa teaches the network node of claim 28, wherein the network node further comprises:

a transmit media access control function **(MAC layer transmitter 22, Figure 1, Hanna)** that processes the transmit data buffered by the transmit FIFO buffer; and

a receive media access control function **(MAC layer receiver 20, Figure 1, Hanna)** that processes the received signals and applying the processed received signals to the receive FIFO buffer.

As to claim 31, Hanna/Taylor/Nagasawa teaches the network node of claim 28, wherein the write buffer in each of the transmit and receive FIFO buffers further comprises:

a plurality of buffer storage locations arranged in rows and columns **("the FIFO memory device 10 memory is organized as Y rows by X columns and the columns are word-wide as well", Column 5, Lines 30-32, Hanna; Note though Hanna teaches the memory array of the FIFO being organized in two dimensions, it would have been obvious to have the buffers of a FIFO organized in two dimensions because it would merely involve applying a known concept of organizing a memory in two dimensions to another type of memory, buffers)**, including first and second columns of buffer storage locations having storage locations in first and second rows; and

sequential logic that controls the write buffer to store a first input data word in a buffer storage location at the first row and the first column, to store a second input data word in a buffer storage location at the second row and the first column **(Note it is obvious to store the words in sequence. After all, a FIFO is being used which is a first-in-first-out buffer)**, and to then forward the first and second input data words to the memory array in an internal write cycle **("the FIFO memory device 10 may also incorporate: an internal clock", Column 4, Lines 65-67, Taylor)**.

As to claim 32, Hanna/Taylor/Nagasawa teaches the network node of claim 31, wherein the write buffer in each of the transmit and receive FIFO buffers further comprises:

a clock input **(Write Clock 36 and Read Clock 38, Figure 1, Taylor)** that receives a periodic clock signal; and

clock circuitry **("the FIFO memory device 10 may also incorporate: an internal clock", Column 4, Lines 65-67, Taylor)** that assigns alternating cycles of the periodic clock signal as internal write and internal read cycles, wherein the sequential logic also controls the write buffer to then store a third input data word in a buffer storage location of the second column responsive to the inputs receiving the third input data word prior to an internal write cycle **("the FIFO memory device 10 memory is organized as Y rows by X columns and the columns are word-wide as well", Column 5, Lines 30-32, Hanna; Note though Hanna teaches the memory array of the FIFO being organized in**

two dimensions, it would have been obvious to have the buffers of a FIFO organized in two dimensions because it would merely involve applying a known concept of organizing a memory in two dimensions to another type of memory, buffers).

As to claim 33, Hanna/Taylor/Nagasawa teaches the network node of claim 28, wherein the read buffer in each of the transmit and receive FIFO buffers further comprises:

an output width converter **(Parallel to Serial Converter 8, Figure 1, Dobson)** that converts double-width output data words read from the memory array into a sequence of output data words; and

an output FIFO **(Transmit FIFO, Figure 1, Dobson)** that is coupled to the output width converter.

As to claim 34, Hanna/Taylor/Nagasawa teaches the network node of claim 33, wherein the read circuitry further comprises an output register **("The input buffer 22 may be implemented in several ways (i.e. as a shift register)", Column 5, Lines 50-51, Taylor; Note it would be obvious to implement the pre-output buffer 48 as a shift register as well)** that presents an output data word received from the output FIFO at the outputs, in combination with a data valid signal **(IBC – indicates the number of valid words in the input buffer, Column 6, Taylor)**, responsive to the read circuitry receiving a read enable signal **("Writing and reading operations are controlled by 'write' and 'read' enables", Column 2, Lines 2-4, Taylor)**.

As to claim 35, Hanna/Taylor/Nagasawa teaches the network node of claim 33, wherein the output FIFO generates a read ready signal responsive to its contents storing a number of output data words exceeding a first threshold **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-16, Taylor; Thus, when the empty flag is cleared, the FIFO will be Allowed to read)**.

4. Claims 37-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanna/Taylor/Nagasawa in view of Yeom.

As to claim 37, Hanna/Taylor/Nagasawa does not appear to teach the network node of claim 28, wherein each packet of data words includes a start-of-packet indicator and an end-of-packet indicator, and wherein each of the transmit and receive FIFO buffers further comprises packet management logic that controls the operation of the memory circuit and that enables the outputting of output data words corresponding to a packet, responsive to detecting the writing of a start-of-packet indicator and an end-of-packet indicator.

Yeom, however, teaches each packet of data words including a start-of-packet indicator and an end-of-packet indicator **("The hardware router 21 checks the ninth bits and detects the start and end of the packet", Column 3, Lines 40-41)** and the transmission of a packet ready signal when the start and end of the packet has been detected **("Once the last byte of the packet is**

written to the transmitting buffer 220, the node 200 sends a packet ready signal, PKTRDY, to the hardware router 21", Column 3, Lines 41-44).

Hanna/Taylor/Nagasawa and Yeom are analogous arts because they both teach buffering.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Hanna/Taylor/Nagasawa and Yeom before him or her, to modify Hanna/Taylor/Dobson to include wherein each packet of data words includes wherein each packet of data words includes a start-of-packet indicator and an end-of-packet indicator, and wherein each of the transmit and receive FIFO buffers further comprises packet management logic that controls the operation of the memory circuit and that enables the outputting of output data words corresponding to a packet, responsive to detecting the writing of a start-of-packet indicator and an end-of-packet indicator because it merely would involve utilizing a known concepts of detecting the start and end of a packet and utilizing a packet ready signal as an enabling signal for enabling the output of data words once both the start and end of the packet has been detected to ensure that whole data words are written instead of partial words.

Therefore, it would have been obvious to combine Yeom with Hanna/Taylor/Nagasawa to obtain the invention as specified in the instant claim.

As to claim 38, Hanna/Taylor/Nagasawa teaches the network node of claim 37, wherein the packet management logic enables the outputting of output data words corresponding to a jumbo packet **("Writing and reading operations**

are controlled by 'write' and 'read' enables", Column 2, Lines 2-4, Taylor; Note the FIFO can store multiple words. Thus, it can store data packets that are multiple words long), responsive to detecting the writing of a start-of-packet indicator and to a packet size indicator indicating that the packet has a length greater than a threshold.

As to claim 39, Hanna/Taylor/Nagasawa teaches the network node of claim 37, wherein the packet management logic maintains a count of the number of packets stored in the memory array **("write row counter" and "read row counter", Column 6 and Column 7, Taylor)**.

As to claim 40, Hanna/Taylor/Nagasawa teaches the network node of claim 39, wherein the packet management logic disables the outputting of output data words, responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-16, Taylor)**.

As to claim 41, Hanna/Taylor/Nagasawa teaches the network node of claim 40, wherein the read buffer further comprises:

an output width converter **(Parallel to Serial Converter 8, Figure 1, Dobson)** that converts double-width output data words read from the memory array into a sequence of output data words;

an output FIFO **(Tx FIFO 7, Figure 1, Dobson)** that is coupled to the output width converter; and

an output register **("The input buffer 22 may be implemented in several ways (i.e. as a shift register)", Column 5, Lines 50-51, Taylor; Note it would be obvious to implement the pre-output buffer 48 as a shift register as well)** that presents an output data word received from the output FIFO at the outputs, in combination with a data valid signal **(IBC – indicates the number of valid words in the input buffer, Column 6, Taylor)**, responsive to the read circuitry receiving a read enable signal **("Writing and reading operations are controlled by 'write' and 'read' enables", Column 2, Lines 2-4, Taylor)**, and wherein the packet management logic controls the output register to disable the outputting of output data words responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored **("The empty flag, therefore prevents reading while empty", Column 2, Lines 15-16, Taylor)**.

Response to Arguments

5. Applicant's arguments with respect to claims 23-41 have been considered but are moot in view of the new ground(s) of rejection necessitated by amendment.

6. Regarding the restriction requirement, Applicant argued in the response on August 20, 2010, "**With respect to item A, separate classification is irrelevant. Regardless of whether these groups can be classified in different groups, a search of the relevant art of the independent claims art would necessarily yield art in the various classifications. It is well-known that Examiners do not perform**

searches for art in 'shoes,' where classification was extremely important, as was the practice before the advent of computers and automated databases. In fact, Examiners conduct word searches on computer databases for patent and non-patent literature references, almost without regard for classification. Based on these word searches of the independent claims, it is clear that art relevant to each group would be yielded. Thus, no 'serious burden' can be established for these closely related groups simply because they can be classified in different classifications", in lines 17 of page 13. Applicant's argument is not persuasive. Though it is true that Examiners no long use "shoes" when performing searches and instead conduct word searches on databases, classification still is a useful and important tool when performing prior art searches. Current databases and classification sizes are much larger than they used to be when "shoes" were used. Mere word searches often times are not powerful enough when searching for prior art due to the size of the databases. A combination of filtration by classification and word search often are needed for performing a proper prior art search. Also, as Applicant's argument points out, MPEP §808.02 states "the examiner must show by appropriate explanation *one of the following*: (A) *Separate classification thereof*... (B) A separate status in the art when they are classifiable together... (C) A different field of search" (emphasis added). Separate classification remains a valid explanation why there would be serious burden on the examiner if the restriction is not required according to the MPEP. Separate classification certainly is not irrelevant. Restriction is maintained. Similar arguments were made with respect to item C.

7. Regarding the restriction requirement, Applicant further argued in the response on August 20, 2010, "**With respect to item B, there is no separate status in the art because a search of the claims of Group II would yield prior art for Group I. Looking to Claims 1 (for example), which Applicant believes to be the broadest claim and which belongs to Group I, all of the limitations of Claims 1 are included (verbatim) in Claim 28... This same type of comparison can be made between Claim 16 (of Group I) and Claim 23 (of Group II). As a result, it is abundantly clear that searches related claims of Group II would result in the same or nearly the same prior art. Therefore, there is clearly no separate status in the art**" from line 18 of page 13 to line 4 of page 15. Even if the claims are determined to be classifiable together, Applicant's argument is not persuasive. When looking at the most comprehensive claims, it is clear that the two groups form separate subjects for inventive effort. Claims 6 and 16 are the most comprehensive claims of group 1. The inventive effort in these claims focus on a buffer and its structure as shown by claim 3 ("the plurality of buffer storage locations are arranged in rows and columns") and claim 17 ("storing the input data word in a write buffer having a plurality of buffer storage locations arranged in rows and columns, each column having first and second buffer storage locations associated with first and second rows, respectively"). Claims 27 and 41 are the most comprehensive claims of group 2. The inventive effort in these claims focus on the data itself, specifically how the packets of data are treated, as shown by claim 26 ("disabling the outputting of output data words, responsive to the outputting of an end-of-packet indication for a packet and to the count indicating that no additional

packets are stored") and claim 41 ("wherein the packet management logic controls the output register to disable the outputting of output data words responsive to the outputting an end-of-packet indication for a packet and to the count indicating no additional packets are stored"), and have separate utility. A search for publications regarding packetizing of data, start-of-packet indicators, and end-of-packet indicators will not yield publications regarding buffers and buffer structures. Thus, there is a separate status in the art.

8. Regarding the objection to claim 38, Applicant's argument is persuasive. The objection is withdrawn.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KRIS RHU whose telephone number is (571)270-1728. The examiner can normally be reached on MTWThF 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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